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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/437,169 | 11/10/1999 | MARK D. RUSTAD | 977.029US1 | 7612 |

21186 7590 06/12/2002

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| EXAMINER |
|---|
| KING, JUSTIN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 06/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.



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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/437,169 | RUSTAD, MARK D. | |
| | Examiner | Art Unit | |
| | Justin I. King | 2181 | |

*-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Claims 18, 30-36, and 62 are objected to as it includes the terminology, "data structure", which is so different from that which is generally accepted in the computer art. The "data structure" is generally meant the logical data arrangement by a database engine.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-2, 4-7, and 30-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al. (U.S. Patent No. 3,845,474) in view of Suzuki et al (U.S. Patent No. 4,151,592).

Lange discloses the multiprocessor system's cache clearing operation. Lange discloses a multiprocessor system with a main memory resource (figure 1, structure 4) and a plurality of entities with cache memory (figure 1, processor 1 and 2, structures 11). Lange discloses a gate (figure 1, structure 6), which is a software controls the access to the main memory resource; Lange's gate blocks processor's request while another processor is already communicating with the main memory resource (column 3, lines 55-60). Lange groups his cache into 4 groups for resetting (column 5, column 6, lines 1-13), and the cache stores the frequently accessed data and its associated address in the main memory resource. Lange discloses a selective cache clearing operation while one of entities accesses the resource (claims 1-11). Lange discloses that it is desired to clear a portion of the cache when its processor starts executing instructions or while the main resource memory is modified by another processor (column 1, lines 11-69, column 2, lines 1-10 and 45-51), such that it is said at least a portion of the cache memory of the at least one entity is not reset when the at least one entity is the same entity that previously had control of the resource, and it is also said that at least a portion of the memory of the at least one entity is selectively reset when the at least one entity is different from an entity that previously had control of the resource. Lange also discloses a system controller (figure 1, structure 3), which controls processors' access to the main memory resource (column 3, lines 40-48). Since Lange's system controller controls processors' access to the main memory resource, it is said that Lange's system controller manages request from the plurality of entities to access the resource; hence, Lange's system controller is equivalent to applicant's claimed manager.

Suzuki discloses a multiprocessor system with one common bus (figure 1, structure 11) and a bus control circuit (figure 1, structure 16). Suzuki's bus control circuit grants processors

for the use of common bus (column 3, lines 5-8). Since Suzuki's bus control circuit grants bus access to each processor, it is said that Suzuki's bus control circuit arbitrates the bus request from the plurality of entities; thus, Suzuki's bus control circuit is equivalent to applicant's claimed arbiter. Suzuki teaches that it is known to one in the computer art to construct a multiprocessor system with one common bus and a bus arbitrator because the common bus provides every processor the direct link to any shared system resource.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time applicant made the invention to adapt Suzuki's teaching into Lange because the common bus provides a direct link between each processor and the shared system resources.

5. Claims 3, 8-29, and 43-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange in view of Suzuki, and in further view of Moreton (U.S. Patent No. 4,035,777).

Referring to claim 3: Moreton discloses a multiprocessor system with integrated circuits (column 1, lines 5-25). Moreton teaches that it is known to one in the computer art to adapt large-scale integrated circuits, medium-scale integrated circuits, or small-scale integrated circuits into a multiprocessor system because the integrated circuits provide necessary interconnections among system components. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Moreton's teaching into Lange and Suzuki because the integrated circuits provide necessary interconnections among system components and expand system's functionalities.

Referring to claims 8-11, 14-16, 19-22, 27-29, 43-44, 46-55, 58-59, 63-66, 71-75, and 77-79: These claims are rejected over Lange in view of Suzuki, and in further view of Moreton as stated above; furthermore, the Lange discloses a communication control unit (figure 1, structure 15), which is a hardware coupled to the processor. "Official Notices" are taken on the followings: It is well known to one in the computer art that, in a multiprocessor system with a master processor or a managing processor, the master processor or the managing processor is responsible to manage and distribute the system resources. Hence, the Lange's communication control unit can be equivalent to the claimed hardware switch mechanism or the claimed lock while it is with the multiprocessor system's master processor. It is also well known to one in the computer art that each processor can equip with L1 cache and L2 cache, which are the primary cache and secondary cache.

Referring to claims 12-13 and 56-57: Claims 12-13 and 56-57 are rejected over Lange in view of Suzuki, and in further view of Moreton as stated above; furthermore, since the Lange's gate is a software that manages the memory access, it is said the Lange's gate is equivalent to the claimed software switch mechanism. An "Office Notice" is taken on the following: E. W. Dijikstra is a well-known professor for his thread-related concept, such as the thread packages and the synchronization primitives.

Referring to claims 16, 26, 45, 60, 70, and 76: These claims are rejected over Lange in view of Suzuki, and in further view of Moreton as stated above; furthermore, the Lange's system controller is equivalent to the claimed communication channel controller.

Referring to claims 17-18, 24-25, 61-62, and 68-69: These claims are rejected over Lange in view of Suzuki, and in further view of Moreton as stated above; furthermore, "Official Notices" are taken on the following: it is known to one in the computer art that the memory can contain software as part of system resource, and it is also known to one in the computer art that this software can be a database with a database structure for data management and storage, furthermore, it is known to one in the computer art that any executable software resource is in binary format.

Referring to claims 23 and 67: Claims 23 and 67 are rejected over Lange in view of Suzuki, and in further view of Moreton as stated above; furthermore, the Lange discloses registers in figure 2's structures 18, 21, 30. An "Official Notice" is taken on the following: In a multiprocessor system with a master processor, Lange's register can be used to store and track the resource usage.

***Conclusion***

6. The prior art made of recorded and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 4,774,625 to Yamanaka: Yamanaka teaches a multiprocessor system with a master processor unit and several slave processor units.

Computer System Architecture, 1982, 2nd edition, authored by M. Morris Mano and published by Englewood Cliffs, N.J., pp 454-462: The Computer System Architecture, as a popular academic textbook, discloses the multiprocessor's operation including the resource management, common bus, bus arbitration, tightly coupled system, loosely coupled system

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephones are unsuccessfully, the examiner's supervisor, Peter Wong can be reached at (703) 305-3477.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.

Justin King
June 10, 2002

PETER WONG
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100